

PATENT

Docket: 00-285

"EXPRESS MAIL" MAILING

LABEL NUMBER EL715231755US

DATE OF DEPOSIT 10/12/2000

I HEREBY CERTIFY THAT THIS PAPER OR
FEE IS BEING DEPOSITED WITH THE UNITED
STATES POSTAL SERVICE "EXPRESS MAIL
POST OFFICE TO ADDRESSEE" SERVICE
UNDER 37 C.F.R. §1.10 ON THE DATE
INDICATED ABOVE AND IS ADDRESSED TO
THE ASSISTANT COMMISSIONER FOR
PATENTS, WASHINGTON, D.C. 20231

MANU KASHYAP

[NAME OF PARALEGAL]

Frame Matching Method

By:

Feng Qian
25851 Majorca Way
Mission Viejo, CA 92692
Citizenship: U.S.

09687700-101200

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to frame based digital communication systems and more particularly to a method for processing frames having a certain size in systems configured for frames having a different size.

Description of the Related Art

Digital data is often communicated in frames, which are groups of digital data that are processed together, as will be further described below. Often, it is desired to send or receive frames having a certain size in systems configured for different sized frames. For example, in the IS2000.2-A standard for code division multiple access (CDMA) communications, encoded symbols at a rate of L symbols per frame must be matched with a transmission scheme that processes N symbols per frame, where N is greater than L. In this case, for any one frame, the L symbols are repeated M times, where M is the smallest integer such that $ML > N$. Then, the ML symbols are reduced to N symbols by deleting (puncturing) P symbols, where $P = ML - N$. There is no appreciable loss of information since in CDMA, many symbols are redundant to provide robust protection against transmission errors; deleting a few redundant symbols will typically not cause any significant problems, especially if the symbols are far apart.

The above mentioned two stage approach has drawbacks. If complex control logic is not used, then it requires unnecessary additional memory to store the ML symbols; in the worst case, this can be almost twice as much memory as would otherwise be required if the actual frame size is only 1 bit shorter than the standard frame size. Moreover, additional data transfer (re-arrangement) is needed because of the two-stage processing.

It would be desirable to improve upon the above mentioned scheme.

SUMMARY OF THE INVENTION

According to the present invention, a frame of digital data with L symbols is matched to a frame with N symbols without (preferably) the need for performing any puncturing. This is performed by making that number of copies of the original L symbols that results in N symbols. In particular, $M = \text{floor}(N/L)$ is computed. $L_2 = N - ML$ is computed. ($L_1 = L - L_2$ where L_1 and L_2 solve the simultaneous equations $L_1 + L_2 = L$ and $L_1 * M + L_2 * (M + 1) = N$). The frame is effectively divided into two mutually exclusive groups of symbols; one group (consisting of L_1 symbols) is copied M times and the other group (consisting of L_2 symbols) is copied $M + 1$ times.

10

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in
5 which:

Figure 1 is a block diagram of a possible digital communication system that includes a frame matching circuit the implements a frame matching method according to
10 the present invention.

Figure 2 is a flow chart of a frame matching method according to the present invention.

While the invention is susceptible to various modifications and alternative forms,
15 specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the
20 appended claims.

DETAILED DESCRIPTION OF THE INVENTION

This specification describes frame matching methods in the context of CDMA
5 systems. However, it will be appreciated that the present invention is not restricted to
CDMA systems.

Figure 1 represents a digital communications system 140 within which the present
invention may be embodied. As shown, the digital system 140 comprises a discrete-time
10 channel 142 interposed between an encoder 144 and a decoder 130. Discrete-time
channel 142 comprises a modulator 146, a channel 148 and a demodulator 150. An
interleaver 145 is interposed between the encoder 144 and the modulator 146. A
deinterleaver 151 is interposed between the decoder 130 and the demodulator 150.
Channel 148 may be a transmission channel or a storage medium being written to and
15 read from. Interleaver 145 receives a digital output signal from a rate matching circuit
147, which in turn receives a digital signal from an encoder 144. The interleaver 145
interleaves this digital output signal over a certain time period, which is usually
predetermined and known as a frame. Modulator 146 serves to translate the digital output
signal from interleaver 145 into signals suitable for channel 148 and thereafter drives the
20 signals across channel 148.

Channel 148 may suffer from interference that corrupts said signals, the
interference possibly taking form in any combination of additive noise, cross channel
interference, multi-path interference, and channel fading. Demodulator 150 serves to
25 receive the signals from channel 148 while minimizing the interference as much as is
practical, and thereafter translate the signals into digital signals for input to deinterleaver
151, which deinterleaves the digital signal and provides it to decoder 130. Discrete-time
channel 142 can thus be viewed as a unit accepting digital input signals and producing

possibly corrupted digital output signals although the present invention is not limited to noisy channels.

Encoder 144 is a convolutional encoder which serves to add redundancy to input data signal 152. The output of the encoder 144 is L symbols per frame, which must be matched with the interleaver 145, which interleaves N symbols per frame, where N is greater than L. This matching is performed by the rate matching circuit 147, which repeats the L symbols of an input frame in such a manner that an N symbol frame is produced.

Figure 2 is a flow chart that describes an embodiment of the matching circuit 147 according to the present invention. In block 198, a frame is received. (It will be appreciated that the frame need not be received all at once and the steps described below may be initiated before the entire frame is received). In block 200, $M = \text{floor}(N/L)$ is computed. In block 202, $L_2 = N - ML$ is computed. ($L_1 = L - L_2$ where L_1 and L_2 solve the simultaneous equations $L_1 + L_2 = L$ and $L_1 * M + L_2 * (M + 1) = N$). As will be described further below, the frame is effectively divided into two mutually exclusive groups of symbols; one group (consisting of L_1 symbols) will be copied M times and the other group (consisting of L_2 symbols) will be copied M+1 times.

The below described steps serially process the symbols, selecting each symbol for inclusion in one group or the other. It will be appreciated that the two groups may be distributed in any manner so long as the totals for each group are L_1 and L_2 respectively at the end of the frame. For example, the first L_1 symbols in a frame could be selected for the first group and the remaining L_2 symbols selected for the second group. According to the preferred embodiment described below, the distribution is such that, at any time in the process, the ratio between A/B is as close to 1 as possible, where A is the total number of symbols that have previously been selected for the first group and B is the

total number of symbols that have previously been selected for the second group. In other words, the groups are selected more or less evenly, according to the ratio L1:L2.

In block 204, two variables, SymbolCnt and RatioCnt are initialized to 0. Block
5 206 is the start of a while loop, which exits at block 220 (and is then further processed by a digital communications system, which, in the case of the system in Figure 1, means it is then interleaved by interleaver 145) when SymbolCnt is equal to L (i.e. it exits when all of the symbols have been processed). Within the while loop, an array NumberOfRepeat is indexed by SymbolCnt; each element in NumberOfRepeat stores the number of times
10 the symbol corresponding SymbolCnt will be multiplied (i.e. either M or M+1 times). For example, if NumberOfRepeat(0) = M, then the 0th symbol will be repeated M times. Specifically, in block 208,, NumberOfRepeat(SymbolCnt) is set equal to M.

In block 210, a variable RatioCnt is set equal to its current value + L2. RatioCnt,
15 as its name implies, essentially tracks the distribution between multiplications by L1 and L2. In block 212, it is determined whether RatioCnt is greater than or equal to L. If so, this means that the current symbol must be repeated M+1 times; thus, in block 214, NumbeOfRepeat(SymbolCnt) is set to M+1 (i.e. its current value M, incremented by 1). Also, RatioCnt must be reduced by L, which is done in block 216. In block 218,
20 SymbolCnt is incremented and the process loops back to block 206.

Conclusion

Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the following
25 claims be interpreted to embrace all such variations and modifications.